I'm not a robot

Reconfigurable digital circuit elementThis article's lead section may be too short to adequately summarize the key points. Please consider expanding the lead to provide an accessible overview of all important aspects of the article. (January 2013)A simplified PAL device. The programmable elements (shown as a fuse) connect both the true and complemented inputs to the AND gates. These AND gates, also known as product terms, are ORed together to form a sum-of-products logic array.A programmable logic device (PLD) is an electronic component used to build reconfigurable digital circuits. Unlike digital logic constructed using discrete logic gates with fixed functions, the function of a PLD is undefined at the time of manufacture. Before the PLD can be used in a circuit it must be programmed to implement the desired function.[1] Compared to fixed logic devices, programmable logic devices simplify the design of complex logic and may offer superior performance.[2] Unlike for microprocessors, programming a PLD changes the connections made between the gates in the device.PLDs can broadly be categorised into, in increasing order of complexity, simple programmable logic devices (SPLDs), comprising programmable array logic, programmable logic array and generic array logic; complex programmable logic devices (CPLDs); and field-programmable gate arrays (FPGAs).In 1969, Motorola offered the XC157, a mask-programmed gate array with 12 gates and 30 uncommitted input/output pins.[3]In 1970, Texas Instruments developed a mask-programmable IC based on the IBM read-only associative memory or ROAM. This device, the TMS2000, was programmed by altering the metal layer during the production of the IC. The TMS2000 had up to 17 inputs and 18 outputs with 8 JK flip-flops for memory. TI coined the term programmable logic array (PLA) for this device.[4]In 1971, General Electric Company (GE) was developing a programmable logic device based on the new programmable read-only memory (PROM) technology. This experimental device improved on IBM's ROAM by allowing multilevel logic. Intel had just introduced the floating-gate UV EPROM so the researcher at GE incorporated that technology. The GE device was the first erasable PLD ever developed, predating the Altera EPLD by over a decade. GE obtained several early patents on programmable logic devices.[5][6][7]In 1973 National Semiconductor introduced a mask-programmable PLA device (DM7575) with 14 inputs and 8 outputs with no memory registers. This was more popular than the TI part but the cost of making the metal mask limited its use. The device is significant because it was the basis for the field programmable logic array produced by Signetics in 1975, the 82S100. (Intersil actually beat Signetics to market but poor yield doomed their part.)[8][9]In 1974 GE entered into an agreement with Monolithic Memories (MMI) to develop a mask-programmable logic device incorporating the GE innovations. The device was named programmable associative logic array or PALA. The MMI 5760 was completed in 1976 and could implement multilevel or sequential circuits of over 100 gates. The device was supported by a GE design environment where Boolean equations would be converted to mask patterns for configuring the device. The part was never brought to market.[10]Main article: Programmable logic arrayIn 1970, Texas Instruments developed a mask-programmable IC based on the IBM read-only associative memory or ROAM. This device, the TMS2000, was programmed by altering the metal layer during the production of the IC. The TMS2000 had up to 17 inputs and 18 outputs with 8 JK flip-flops for memory. TI coined the term programmable logic array for this device.[4]A programmable logic array (PLA) has a programmable AND gate array, which links to a programmable OR gate array, which can then be conditionally complemented to produce an output. A PLA is similar to a ROM concept, however a PLA does not provide full decoding of a variable and does not generate all the minterms as in a ROM.The programmable logic sequencer (PLS/FPLS) is similar to a PLA, but with integral registered outputs using a number of flip-flops to allow creation of some state machines. Signetics introduced the first FPLS in 1979.[11]Main article: Programmable array logicPAL devices have arrays of transistor cells arranged in a "fixed-OR, programmable-AND" plane used to implement "sum-of-products" binary logic equations for each of the outputs in terms of the inputs and either synchronous or asynchronous feedback from the outputs.MMI introduced a breakthrough device in 1978, the programmable array logic or PAL. The architecture was simpler than that of Signetics' FPLA because it omitted the programmable OR array. This made the parts faster, smaller and cheaper. They were available in 20-pin 300-mil DIP packages, while the FPLAs came in 28-pin 600-mil packages. The PAL Handbook demystified the design process. The PALASM design software (PAL assembler) converted the engineers' Boolean equations into the fuse pattern required to program the part. The PAL devices were soon second-sourced by National Semiconductor, Texas Instruments and AMD.After MMI succeeded with the 20-pin PAL parts, AMD introduced the 24-pin 22V10 PAL with additional features. After buying out MMI (1987), AMD spun off a consolidated operation as Vantis, and that business was acquired by Lattice Semiconductor in 1999.Main article: Generic array logicLattice GAL 16V8 and 20V8. These are 35 nanosecond devices.An improvement on the PAL was the generic array logic device, or GAL, invented by Lattice Semiconductor in 1985. This device has the same logical properties as the PAL but can be erased and reprogrammed. The GAL is very useful in the prototyping stage of a design when any bugs in the logic can be corrected by reprogramming. GALs are programmed and reprogrammed using a PAL programmer, or, in the case of chips that support it, by using the in-circuit programming technique.Lattice GALs combine CMOS and electrically erasable (E2) floating gate technology for a high-speed, low-power logic device. A similar device called a PEEL (programmable electrically erasable logic) was introduced by the International CMOS Technology (ICT) corporation.Sometimes GAL chips are referred as simple programmable logic device (SPLD), analogous to complex programmable logic device (CPLD) below.Main article: Complex programmable logic devicePALs and GALs are available only in small sizes, equivalent to a few hundred logic gates. For bigger logic circuits, complex PLDs or CPLDs can be used. These contain the equivalent of several PALs linked by programmable interconnections, all in one integrated circuit. CPLDs can replace thousands, or even hundreds of thousands, of logic gates.Some CPLDs are programmed using a PAL programmer, but this method becomes inconvenient for devices with hundreds of pins. A second method of programming is to solder the device to its printed circuit board, then feed it with a serial data stream from a personal computer. The CPLD contains a circuit that decodes the data stream and configures the CPLD to perform its specified logic function. Some manufacturers, such as Altera and Atmel (now Microchip), use JTAG to program CPLDs in-circuit from .JAM files.Main article: Field-programmable gate arrayWhile PALs were being developed into GALs and CPLDs (all discussed above), a separate stream of development was happening. This type of device is based on gate array technology and is called the field-programmable gate array (FPGA). Early examples of FPGAs are the 82S100 array, and 82S105 sequencer, by Signetics, introduced in the late 1970s. The 82S100 was an array of AND terms. The 82S105 also had flip-flop functions.(Remark: 82S100 and similar ICs from Signetics have PLA structure, AND-plane + OR-plane.)FPGAs use a grid of logic gates, and once stored, the data doesn't change, similar to that of an ordinary gate array. The term field-programmable means the device is programmed by the customer, not the manufacturer. FPGAs and gate arrays are similar but gate arrays can only be configured at the factory during fabrication.[12][13][14] FPGAs are usually programmed after being soldered down to the circuit board, in a manner similar to that of larger CPLDs. In most larger FPGAs, the configuration is volatile and must be re-loaded into the device whenever power is applied or different functionality is required. Configuration is typically stored in a configuration PROM, EEPROM or flash memory.[15] EEPROM versions may be in-system programmable (typically via JTAG).The difference between FPGAs and CPLDs is that FPGAs are internally based on look-up tables (LUTs), whereas CPLDs form the logic functions with sea-of-gates (e.g. sum of products). CPLDs are meant for simpler designs while FPGAs are meant for more complex designs. In general, CPLDs are a good choice for wide combinational logic applications, whereas FPGAs are more suitable for large state machines such as microprocessors.An EPLD from Cypress in a PLCC-packageUsing the same technology as EPROMs, EPLDs have a quartz window in the package that allows them to be erased on exposure to UV light.[16][17]Using the same technology as EEPROMs, EEPLDs can be erased electrically.[16][17]An erasable programmable logic device (EPLD) is an integrated circuit that comprises an array of PLDs that do not come pre-connected; the connections are programmed electrically by the user. Most GAL and FPGA devices are examples of EPLDs.[citation needed]These are microprocessor circuits that contain some fixed functions and other functions that can be altered by code running on the processor. Designing self-altering systems requires that engineers learn new methods and that new software tools be developed.PLDs are being sold now that contain a microprocessor with a fixed function (the so-called core) surrounded by programmable logic. These devices let designers concentrate on adding new features to designs without having to worry about making the microprocessor work. Also, the fixed-function microprocessor takes less space on the chip than a part of the programmable gate array implementing the same processor, leaving more space for the programmable gate array to contain the designer's specialized circuits.A PLD is a combination of a logic device and a memory device. The memory is used to store the pattern that was given to the chip during programming. Most of the methods for storing data in an integrated circuit have been adapted for use in PLDs. These include:Silicon antifusesSRAMEPROM or EEPROM memory cellsFlash memorySilicon antifuses are connections that are made by applying a voltage across a modified area of silicon inside the chip. They are called antifuses because they work in the opposite way to normal fuses, which begin life as connections until they are broken by an electric current.SRAM, or static RAM, is a volatile type of memory, meaning that its contents are lost each time the power is switched off. SRAM-based PLDs therefore have to be programmed every time the circuit is switched on. This is usually done automatically by another part of the circuit.An EPROM memory cell is a MOSFET (metal-oxide-semiconductor field-effect transistor, or MOS transistor) that can be switched on by trapping an electric charge permanently on its gate electrode. This is done by a PAL programmer. The charge remains for many years and can only be removed by exposing the chip to strong ultraviolet light in a device called an EPROM eraser.Flash memory is non-volatile, retaining its contents even when the power is switched off. It is stored on floating-gate MOSFET memory cells, and can be erased and reprogrammed as required. This makes it useful in PLDs that may be reprogrammed frequently, such as PLDs used in prototypes. Flash memory is a kind of EEPROM that holds information using trapped electric charges similar to EPROM. Consequently, flash memory can hold information for years, but possibly not as many years as EPROM.As of 2005, most CPLDs are electrically programmable and erasable, and non-volatile. This is because they are too small to justify the inconvenience of programming internal SRAM cells every time they start up, and EPROM cells are more expensive due to their ceramic package with a quartz window.Many PAL programming devices accept input in a standard file format, commonly referred to as 'JEDEC files'. They are analogous to software compilers. The languages used as source code for logic compilers are called hardware description languages, or HDLs.[1]PALASM, ABEL and CUPL are frequently used for low-complexity devices, while Verilog and VHDL are popular higher-level description languages for more complex devices. The more limited ABEL is often used for historical reasons, but for new designs, VHDL is more popular, even for low-complexity designs.For modern PLD programming languages, design flows, and tools, see FPGA and reconfigurable computing.A device programmer is used to transfer the Boolean logic pattern into the programmable device. In the early days of programmable logic, every PLD manufacturer also produced a specialized device programmer for its family of logic devices. Later, universal device programmers came onto the market that supported several logic device families from different manufacturers. Today's device programmers usually can program common PLDs (mostly PAL/GAL equivalents) from all existing manufacturers. Common file formats used to store the Boolean logic pattern (fuses) are JEDEC, Altera POF (programmable object file), or Xilinx BITstream.[18]Complex programmable logic device (CPLD)Field-programmable gate array (FPGA)Macrocell arrayProgrammable array logic (PAL)^ a b Horowitz, Paul; Hill, Winfield (2015). Horowitz P., Hill W. - The Art of Electronics. New York. p.764. ISBN978-0-521-80926-9.{{cite book}}: CS1 maint: location missing publisher (link)^ Holdsworth, B.; Woods, R. C. (2003). Digital Logic Design (4thed.). Elsevier. ISBN978-0-7506-4582-9.^ Motorola Semiconductor Data Book, Fourth Edition. Motorola Inc. 1969. p.IC-73.^ a b Andres, Kent (October 1970). A Texas Instruments Application Report: MOS programmable logic arrays. Texas Instruments. Bulletin CA-158. Report introduces the TMS2000 and TMS2200 series of mask programmable PLAs.^ Greer, David L. Electrically Programmable Logic Circuits US Patent 3,818,452. Assignee: General Electric, Filed: April 28, 1972, Granted: June 18, 1974^ Greer, David L. Multiple Level Associative Logic Circuits US Patent 3,816,725. Assignee: General Electric, Filed: April 28, 1972, Granted: June 11, 1974^ Greer, David L. Segmented Associative Logic Circuits US Patent 3,849,638. Assignee: General Electric, Filed: July 18, 1973, Granted: November 19, 1974^ "Semiconductors and IC's: FPLA". EDN. 20 (13). Boston, MA: Cahners Publishing: 66. July 20, 1975. Press release on Intersil IM5200 field programmable logic array. Fourteen inputs pins and 48 product terms. Avalanched-induced-migration programming. Unit price was $37.50^ "FPLA's give quick custom logic". EDN. 20 (13). Boston, MA: Cahners Publishing: 61. July 20, 1975. Press release on Signetics 82S100 and 82S101 field programmable logic arrays. Fourteen inputs pins, 8 output pins and 48 product terms. NiCr fuse link programming.^ Pellerin, David; Michael Holley (1991). Practical Design Using Programmable Logic. Prentice-Hall. p.15. ISBN0-13-723834-7.^ Alford, Roger C. (1989). Programmable Logic Designer's Guide. Howard W. Sams. pp.6769. ISBN0-672-22575-1. The registers can be dynamically or permanently configured as D, J-K, or T flip-flops, because of the flexibility offered by the inclusion of the "M" inverters (M0-M5). The outputs of the registers are fed back into the AND-array before reaching the tri-state output buffers, allowing for Mealy and Moore state machine development.^ Dorf, Richard C. (3 October 2018). Electronics, Power Electronics, Optoelectronics, Microwaves, Electromagnetics, and Radar. CRC Press. ISBN978-1-4200-0315-4.^ Vahid, Frank; Givargis, Tony D. (17 October 2001). Embedded System Design: A Unified Hardware / Software Introduction. John Wiley & Sons. ISBN978-0-471-38678-0.^ Chen, Wai-Kai (3 October 2018). The VLSI Handbook. CRC Press. ISBN978-1-4200-0596-7.^ "Using Flash Memory to Configure FPGAs" (PDF). Altera. Retrieved 2024-08-21.^ a b Tertulien Ndjountche."Digital Electronics 2: Sequential and Arithmetic Logic Circuits".2016.p. 224.^ a b Clive Maxfield."The Design Warrior's Guide to FPGAs".2004.p. 20^ PLD File FormatsWikibooks has a book on the topic of: Programmable LogicWikimedia Commons has media related to Programmable logic devices."PLD Tools Creating SVF, JAM, STAPL and other formats". JTAG / boundary-scan. Corelis. Dec 1, 2010. Archived from the original on March 18, 2012. Retrieved July 18, 2011."FPGAs and CPLDs". Lattice Semiconductor.Retrieved from " circuit designs core components that offer adaptability and reconfigurability are programmable array logic (PAL) and programmable logic array (PLA). Engineers can effectively build and optimize digital systems thanks to these devices vital role in implementing complex logic operations.We will look at the distinctions between PAL and PLA, as well as their functional principles, benefits, and common applications, in this post. We will contrast PAL and PLA as well, demonstrating how they differ in terms of their structural makeup, logical prowess, level of design complexity, and performance requirements. Designers will be better equipped to choose the best device for their particular application if they are aware of these distinctions.In order to fully grasp the benefits and advantages of PAL and PLA in these situations, we will also examine how they are applied to various types of logic circuits, including combinational and sequential circuits. We will also talk about PAL and PLA technology developments and how they affect circuit design and application.You will have a thorough understanding of PAL and PLA by the end of this article, enabling you to choose how to use them in digital circuit design. So lets start by going over the fundamentals of PAL and PLA and their importance in contemporary electronics.Image CreditDefinition: PAL (Programmable Array Logic) is a type of programmable logic device that consists of an array of programmable AND gates followed by a fixed OR gate.Architecture: PAL is composed of three main components: an input matrix, an output matrix, and a programmable OR array.Input Matrix: The input matrix consists of programmable AND gates that allow for the combination of input signals. These gates are programmable, meaning their connections can be configured to create different logic functions.Output Matrix: The output matrix consists of a fixed OR gate that combines the outputs from the programmable AND gates in the input matrix. The output matrix provides the final logic function of the PAL.Programmable OR Array: The programmable OR array allows for the connection of various inputs to different OR gates in the output matrix. This enables the implementation of complex logic functions.Working Principle: The input and output matrices are programmed using a particular hardware programming language or software tools when designing with a PAL. The programming sets up the AND gates and OR gates connections to carry out the specified logic function.Components of PALProgrammable AND Gates: The programmable AND gates in the input matrix can be programmed to connect specific inputs to generate the desired logical expressions.Fixed OR Gate: The fixed OR gate in the output matrix combines the outputs from the programmable AND gates to produce the final output signal.Programming Interface: PAL devices are typically programmed using specialized hardware programmers or software tools that provide the necessary interface to configure the interconnections of the gates.Advantages:Flexibility: PAL devices offer a high degree of flexibility since the interconnections of the AND gates can be easily programmed to implement various logic functions.Cost-Effectiveness: PALs are generally more cost-effective compared to other programmable logic devices due to their simpler architecture.Compact Size: PALs are available in small form factors, making them suitable for applications with limited space requirements.Disadvantages:Limited Complexity: PALs have limitations in implementing complex logic functions compared to other programmable logic devices like CPLDs (Complex Programmable Logic Devices) or FPGAs (Field-Programmable Gate Arrays).Fixed OR Gate: The fixed OR gate restricts the PALs ability to perform more advanced logic functions that require complex combinations of signals.PALs are commonly used in various digital circuit applications, including:Data Encoding and Decoding: PALs can be used to encode or decode data signals in applications such as communication systems.Code Conversion: PALs can be utilized to convert between different coding schemes, such as binary to Gray code conversion.Address Decoding: PALs are often employed in memory systems to decode addresses and enable the selection of specific memory locations.Arithmetic Logic Units (ALUs): PALs can be used to implement ALUs in processors, performing arithmetic and logic operations.Definition: A programmable AND array and a programmable OR array make up a digital circuit known as a programmable logic array (PLA), which enables variable logic implementation.Architecture: A PLA typically comprises two main components:Programmable AND array: This section consists of a matrix of programmable AND gates, where inputs can be combined using various logic functions such as AND, OR, NAND, NOR, etc. The outputs of these gates are fed into the OR array.Programmable OR array: The outputs from the AND array are connected to a programmable OR array, which combines the signals using OR logic operations to produce the final output.Working principle: The AND and OR arrays are programmed in a PLA in order to implement particular logic operations. The circuits inputs are connected to the inputs of the AND array, and the arrays outputs are connected to the inputs of the OR array. The needed logic functions can be created by programming the relevant connections and values in the AND and OR arrays.Components of a PLA:Input lines: These are the input signals to the PLA, which can be either high (1) or low (0) logic levels.Programmable AND array: The matrix of programmable AND gates, which allows for combining inputs using various logic functions.Programmable OR array: The array of programmable OR gates, combines the outputs from the AND array to generate the final output.Output lines: These are the output signals produced by the PLA, representing the desired logic function.Advantages:Flexibility: PLA offers high flexibility in implementing complex logic functions due to its programmable nature.Compactness: PLA designs can be more compact than alternative implementations for certain logic functions, reducing circuit complexity and size.Reduced power consumption: Compared to other programmable logic devices, PLA can consume less power, especially when optimized for specific applications.Disadvantages:Limited scalability: PLA designs can become cumbersome and complex for larger logic functions, limiting their scalability.Longer propagation delays: PLA may have longer propagation delays due to the cascading of multiple AND and OR gates, which can affect the overall circuit speed.Higher design effort: Designing a PLA circuit requires careful consideration of the input equations and programming the AND and OR arrays, which can be time-consuming.Control unit design in microprocessors: PLA is commonly used to implement the control logic in microprocessors, enabling efficient instruction decoding and sequencing.Digital signal processing: PLA can be employed in applications such as image processing, audio processing, and communication systems to implement various signal processing algorithms.Data compression and encryption: PLA circuits are utilized in data compression algorithms, encryption schemes, and error detection/correction techniques.Complex combinatorial logic: PLA finds applications in designs requiring complex combinatorial logic functions, such as pattern matching, code conversion, and protocol handling.PAL (Programmable Array Logic):PAL consists of an array of AND gates followed by a fixed OR gate.The output of each AND gate is connected to the input of the OR gate.The connections between inputs and AND gates are programmable using a fuse or anti-fuse technology.PLA (Programmable Logic Array):PLA consists of an array of programmable AND gates followed by programmable OR gates.The inputs of the AND gates and the outputs of the OR gates are programmable through a matrix of fuses or anti-fuses.The number of inputs and outputs in a PLA can vary based on the specific design.PAL:PAL provides a limited number of inputs and outputs, which restricts the complexity of the logic functions it can implement.Due to the fixed OR gate structure, PALs are generally suited for simpler logic functions.PALs offer high flexibility in terms of reprogramming the connections between inputs and AND gates.PLA:PLA offers greater flexibility and higher logic capacity compared to PAL.With the ability to program both the AND gates and OR gates, PLA can implement more complex logic functions.PLA allows for a wider range of input and output configurations, making it suitable for a broader range of applications.PAL:PALs have simpler architecture, resulting in lower design complexity.The reduced complexity often leads to lower manufacturing costs for PAL devices.However, PALs may require additional external logic components to implement more complex functions, which can increase overall system cost.PLA:PLAs flexibility and larger logic capacity make it capable of implementing complex functions without the need for additional external components.The increased logic capacity and flexibility can result in higher design complexity and manufacturing costs compared to PALs.PAL:PALs typically have faster propagation delays and shorter routing paths due to their simpler structure.The reduced complexity allows for faster signal routing and quicker response times in PAL-based circuits.PLA:PLAs more complex structure and larger logic capacity may introduce longer propagation delays and increased signal routing complexity.However, advancements in technology have minimized the performance differences between PAL and PLA in modern designs.PALs are generally preferred when the logic functions are relatively simple, and flexibility in reprogramming is required.PLA is a better choice for applications that demand more complex logic functions, higher logic capacity, and a wider range of input/output configurations.Cost considerations, performance requirements, and design complexity also play a significant role in selecting between PAL and PLA architectures.By understanding the structural differences, logic capabilities, design complexity, performance factors, and design trade-offs between PAL and PLA, designers can make informed decisions regarding their choice of programmable logic devices for different applications.Use cases and advantages of PAL:PALs are commonly used in applications where the logic functions are fixed and well-defined, such as in address decoding circuits and data multiplexers.PALs offer a higher density of gates, allowing for more complex logic functions to be implemented in a smaller physical space.Example: In a microprocessor, a PAL can be used for decoding the address bus to select specific memory locations or peripheral devices. This enhances the overall performance and functionality of the microprocessor.Use cases and advantages of PLA:PLAs are suitable for applications that require flexible logic functions and can benefit from on-the-fly reprogramming capabilities.PLAs excel in applications where frequent changes in logic functions are expected or where customized logic functions need to be implemented.Example: In a complex control system, a PLA can be used to implement a state machine that controls the sequencing and timing of various operations. The ability to reprogram the PLA allows for modifications and updates to the control logic without the need for hardware changes.Use cases and advantages of PAL:PALs can be used in sequential circuits where the feedback path is limited and the number of flip-flops required is relatively small.PALs offer a faster propagation delay compared to PLAs, making them suitable for applications with tight timing requirements.Example: In a counter circuit, a PAL can be used to implement the next state logic that determines the sequence of the counter. This enables efficient counting and control operations.Use cases and advantages of PLA:PLAs are well-suited for sequential circuits with complex feedback paths and a large number of flip-flops.PLAs provide greater flexibility in designing sequential circuits with multiple state transitions and complex control logic.Example: In a digital communication system, a PLA can be used to implement the encoding and decoding algorithms for error correction, allowing for efficient data transmission and reliable communication.Use cases and advantages of PAL:PALs are commonly used in embedded systems where space is a critical factor and the logic functions are fixed and well-defined.PALs offer a cost-effective solution for implementing standard and repetitive logic functions in large-scale integrated circuits.Example: In a digital signal processor (DSP), a PAL can be used for implementing arithmetic and logic functions, enabling efficient data processing and manipulation.Use cases and advantages of PLA:PLAs find applications in complex digital systems where the logic functions are subject to changes and customization.PLAs provide the flexibility to adapt and modify the logic functions without the need for significant hardware changes.Example: In a reconfigurable computing system, a PLA can be used for implementing custom logic functions based on the specific computational requirements of different applications, allowing for improved performance and versatility.By utilizing PALs and PLAs effectively in specific applications, designers can optimize the performance, flexibility, and cost-efficiency of their digital circuits.Key elements in the design of digital circuits are PAL (Programmable Array Logic) and PLA (Programmable Logic Array). PLAs provide more versatility and support for complicated logic functions, but PALs offer simplicity, small size, and faster performance.Design complexity, performance requirements, cost, and required flexibility are a few of the aspects that designers must take into account while deciding between PAL and PLA. PALs work well for more compact and straightforward designs, whereas PLAs flourish in systems and projects that are bigger in scope and have more complex logic requirements.Digital circuit design is constantly evolving, with improvements in performance, density, and programmability being driven by PAL and PLA technology advancements.In conclusion, PALs and PLAs are essential for implementing logic operations, and knowing how they differ from one another enables designers to make wise choices. The creation of sophisticated electronic systems is made possible by these programmable logic circuits. Share copy and redistribute the material in any medium or format for any purpose, even commercially. Adapt remix, transform, and build upon the material for any purpose, even commercially. The licensor cannot revoke these freedoms as long as you follow the license terms. Attribution You must give appropriate credit , provide a link to the license, and indicate if changes were made . You may do so in any reasonable manner, but not in any way that suggests the licensor endorses you or your use. ShareAlike If you remix, transform, or build upon the material, you must distribute your contributions under the same license as the original. No additional restrictions You may not apply legal terms or technological measures that legally restrict others from doing anything the license permits. You do not have to comply with the license for elements of the material in the public domain or where your use is permitted by an applicable exception or limitation . No warranties are given. The license may not give you all of the permissions necessary for your intended use. For example, other rights such as publicity, privacy, or moral rights may limit how you use the material. Share copy and redistribute the material in any medium or format for any purpose, even commercially. Adapt remix, transform, and build upon the material for any purpose, even commercially. The licensor cannot revoke these freedoms as long as you follow the license terms. Attribution You must give appropriate credit , provide a link to the license, and indicate if changes were made . You may do so in any reasonable manner, but not in any way that suggests the licensor endorses you or your use. ShareAlike If you remix, transform, or build upon the material, you must distribute your contributions under the same license as the original. No additional restrictions You may not apply legal terms or technological measures that legally restrict others from doing anything the license permits. You do not have to comply with the license for elements of the material in the public domain or where your use is permitted by an applicable exception or limitation . No warranties are given. The license may not give you all of the permissions necessary for your intended use. For example, other rights such as publicity, privacy, or moral rights may limit how you use the material. In this chapter, we will talk about Programmable Logic Array (PLA), its block diagram, and applications. The programmable logic array (PLA) is a type of programmable logic device (PLD). Historically, PLA is the first PLD device. It contains an array/matrix of AND and OR gates whose configuration is done as per the needs of applications.In a PLA, a set of fusible links is used to establish or remove the contact of a literal in the AND operation or contact of a product term in the OR operation. Therefore, a PLA is a type of PLD that allows both AND matrix and OR matrix to program.In digital electronics, PLAs are used to design and implement a variety of complex combinational circuits. However, some PLAs also have a memory element, hence they can be used to implement sequential circuits as well.Block Diagram of PLAA programmable logic array (PLA) is a type of fixed architecture programmable logic device (PLD) which consists of programmable AND and OR gates. A PLA contains a programmable AND array which is followed by a programmable OR array.The block diagram of the PLA is shown in the following figure It consists of the following main components Input BufferThe input buffer is used in PLA to avoid the loading effect on the source that drives the inputs.AND Array/Matrix The AND array/matrix is used in PLA to generate the product terms.OR Array/Matrix In a PLA, the OR array/matrix is used to generate the desired output. This is done by Oring the product terms to produce the sum terms.Invert/Non-Invert Matrix It is a buffer used in PLAs to set the output to active-high or active-low.Output Buffer This buffer is used at the output side. It is mainly provided to increase the driving capability of the programmable logic array (PLA). In the field of digital electronics, the PLAs are extensively used for designing combinational logic circuits. The greatest advantage of designing combinational circuits using PLAs is that PLA consist of programmable AND and OR arrays which allows to implement custom desired logic functions.The step-by-step procedure to design a combinational logic circuit using PLAs is explained below Step 1 Develop a PLA program table that shows the inputs, product terms, and outputs.Step 2 Design the AND matrix that can generate the desired product terms.Step 3 Design the OR matrix that can generate the desired output.Step 4 Design the invert/non-invert matrix to set the active-low or active-high output.Step 5 Finally, program the PLA by utilizing the PLA program table.Let us understand this process of combinational circuit design using PLA with the help of an example.ExampleDesign a full-adder circuit using programmable logic array (PLA).SolutionA full-adder consists of three-inputs and two outputs. Since it has 3 inputs, thus there are total 8 product terms which are given in the following truth table of the full adder InputsOutputsABCinSCout00000000110010100110110010101011100111111From this truth table, the output sum (S) and the output carry (Cout) are given by,$$\mathrm{S \: = \: \sum \: m(1,2,4,7)}$$$$\mathrm{C_{out} \: = \: \sum \: m(3,5,6,7)}$$Thus, their Boolean expressions will be,$$\mathrm{S \: = \: \overline{A} \: B \: \overline{C_{in}} \: + \: \overline{A} \: \overline{B} \: C_{in} \: + \: A \: \overline{B} \: \overline{C_{in}} \: + \: A \: B \: C_{in}}$$$$\mathrm{C_{out} \: = \: A \: B \: + \: B \: C_{in} \: + \: A \: C_{in}}$$From these two Boolean expressions, we can see that there are seven product terms and two sum terms. The PLA program table for this full-adder circuit is shown below Sr.NoProduct TermsInputsOutputsABCinSCout1$\mathrm{\overline{A} \: B \: \overline{C_{in}}}$0101-2$\mathrm{\overline{A} \: \overline{B} \: C_{in}}$0011-3$\mathrm{A \: \overline{B} \: \overline{C_{in}}}$1001-4$\mathrm{A \: B \: C_{in}}$1111-5$\mathrm{A \: B }$11--16$\mathrm{B \: C_{in}}$-11-17$\mathrm{A \: C_{in}}$1-1-1TTIn this PLA program table, "1" stands for the connection and "-" stands for the absence of the product term in the output. "T" that stands for true and it represents the active-high output.The PLA circuit diagram of the full-adder is shown in the following figure.This example illustrates the complete step-by-step procedure to implement a combinational logic circuit using PLA.Advantages of PLAsThe following are some key advantages of Programmable Logic Arrays (PLAs) that make them indispensable in the field of digital electronics PLAs provide flexibility in terms of design and implementation of a variety of digital logic operations. PLAs can be used to implement custom logic functions required to fulfil the needs of different applications.PLAs also minimize the time required to design and develop a new digital circuit or system.PLAs provide a less expensive way of implementing highly complex digital logic functions. PLAs eliminate the need of discrete components to implement a logic function, hence they result in space efficiency.Since PLAs are programmable, they can be modified on their designs without re-fabricating the entire circuit.Disadvantages of PLAsHowever, PLAs offer several advantages as discussed above. But they also have some disadvantages which are listed below For a large number of inputs and outputs, PLAs are highly complex to design and implement. Being a fixed architecture device, PLAs have limited performance in terms of speed and processing power.A PLA is generally optimized for a specific application, as it has a fixed number of AND gates and OR gates. This constraint disallows the designers to implement highly complex logic functions with the same PLA.Program a PLA is a time consuming and complex process.Applications of PLAsProgrammable Logic Arrays (PLAs) are widely used in various applications across different fields. The following are some common applications of PLAs PLAs are used in the field of digital signal processing to implement various logical functions, such as filtering, convolution, Fourier transformation, etc.In control systems, PLAs are used to implement control logic functions of various components like feedback, PID controllers, state machines, etc.PLAs are used to perform different types of arithmetic operations like addition, subtraction, multiplication, and division.PLAs also find their application in the field data compression and encryption technologies. PLAs are used in digital communication systems and networking equipment to implement algorithms for protocol handling, packet processing, error detection and correction, and more.PLAs are also used in different measuring instruments such as digital oscilloscopes, protocol analyzers, logic analyzer, etc.ConclusionA PLA is nothing but a kind of digital logic device used to implement complex digital functions without need of discrete components like AND gates, OR gates, etc. In this chapter, we explained the basics and applications of programmable logic arrays (PLAs). Programmable Logic Array is a type of PLD, which has both programmable AND array and programmable OR array.In a combinational circuit, because of dont care conditions, not all the minterms are used. In the case of PROM, where the AND matrix is fixed, all the product terms are not used. This makes the PROM PLD to poor utilization.If the number of dont care conditions is more, then PROM will be not suitable for efficient usage. Hence, it is very necessary to switch to a more economical device, called Programmable Logic Array(PLA).PLA is somewhat similar to the PROM. Both have a programmable OR array, but in PLA, there is a modification in the AND array. PLA does not generate all the minterms, rather depending on the function, the required product terms can be obtained.The following figure shows the block diagram of programmable logic array.It consists of n-inputs, inverters, input buffer, m-outputs and an output buffer. Both AND and OR array have fuses at the inputs, which makes them to be programmable.The AND matrix or array produces product terms, through the AND gates, which are ORed to get the required function.In PLA, the input buffers are used to limit the loading of the sources that drive the inputs. The driving capacity of PLA device is increased with the help of output buffers.An example of PLA circuit of a combinational circuit is shown below. As you can observe from the circuit diagram, it is similar to the PROM circuit, except that the AND array consists of fuses, to program according to the user requirements.The sequential circuits can also be implemented with PLA. For such implementation, flip-flops are also provided at each output of the OR matrix.Now let us look at some examples of realization of combinational circuit using PLA.In this example, lets see how to realize the Boolean expression X = AB + ABC + BC and Y = BC + ABC + ABC using Programmable Logic Array.For the given problem, there are three inputs(A, B, C) and two outputs(X, Y). The complement of three inputs are obtained through NOT gates. Thus the realization has six input lines(input with its complement).The given expression has six product terms and so the fuses are placed in the corresponding literals to obtain the product terms.Two OR gate arrays are used at the output to realize the the two functions. The fuses are placed at the corresponding product terms for each Boolean function.For this example, let us realize a boolean functions F1(A, B, C) = m(1, 3, 6, 7) and F2(A, B, C) = m(0, 2, 4, 5) using PLA.Here, two boolean functions are given in terms of minterms. To obtain the expression, the given function is implemented using Karnaugh map.Thus for the two obtained expressions, the PLA circuit is realized. For which, there are three inputs(A, B, C) and two outputs(F1, F2). In the obtained expressions, there are four product terms and so four AND gate array is used. Two OR gates are used to generate the two boolean fuctions.The realization of the given Boolean function is drawn below.,the free encyclopedia that anyone can edit.110,144 active editors 7,022,868 articles in EnglishSiriusA with SiriusB, a white dwarf, indicated by the arrowA white dwarf is a stellar core remnant composed mostly of electron-degenerate matter, supported against its own gravity only by electron degeneracy pressure. A white dwarf is very dense: in an Earth sized volume, it contains a mass comparable to the Sun. What light it radiates is from its residual heat. White dwarfs are thought to be the final evolutionary state of stars whose mass is insufficient for them to become a neutron star or black hole. This includes more than 97% of the stars in the Milky Way. After the hydrogen-fusing period of such a main-sequence star ends, it will expand to a red giant and shed its outer layers, leaving behind a core which is the white dwarf. Very hot when it forms, this cools as it radiates its energy until its material begins to crystallize into a cold black dwarf. The oldest known white dwarfs still radiate at temperatures of a few thousand kelvins, which establishes an observational limit on the maximum possible age of the universe. (Fullarticle...)Recently featured: Battle of GroixScott CarpenterJohann Reinhold ForsterArchiveBy emailMore featured articlesAboutA Royal 10 typewriter... that a Royal 10 (pictured) used in the music video for "Fortnight" caused an interest in typewriters among Swifties?... that the Brazilian government advocated the use of COVID kits, which contained a drug used to treat head lice?... that Brave Bunnies was among the children's series streamed ad-free on Sunflower TV for Ukrainian refugees?... that it took more than two years after the Romans invaded Africa in 2104BC for them to completely defeat the Carthaginians?... that the Pittsburgh Post-Gazette reported that "half of the residents of Mount Desert Island, Maine, are convinced they are millionaires since the body of Karl N. Mellon" was discovered?... that AiScReam's recent debut song "Ai Scream!" went viral on social media?... that Laura LeRoy Travis was the first woman at the University of Delaware to coach a men's sports team?... that the screenplay for Smashing Frank was developed from an assignment in a filmmaking course?... that the iconic 1937 photograph At the Time of the Louisville Flood identifiably depicts neither Louisville nor the flood?ArchiveStart a new articleNominate an articleVera Rubin ObservatoryThe Vera C. Rubin Observatory (pictured) in Chile releases the first light images from its new 8.4-metre (28ft) telescope.In basketball, the Oklahoma City Thunder defeat the Indiana Pacers to win the NBA Finals.A terrorist attack on a Greek Orthodox church in Damascus, Syria, kills at least 25 people.The United States conducts military strikes on three nuclear facilities in Iran.In rugby union, the Crusaders defeat the Chiefs to win the Super Rugby Pacific final.Ongoing: Gaza warIranIsrael warRussian invasion of UkrainetimelineSudanese civil wartimelineRecent deaths: Anne BurrellFrederick W. SmithRon TaylorMohammad KazemiMarita Camacho QuirsKim WoodburnNominate an articleJune 24: Jaanipev in EstoniaJulia Gillard1374 An outbreak of dancing mania, in which crowds of people danced themselves to exhaustion, began in Aachen (in present-day Germany) before spreading to other parts of Europe.1717 The first Grand Lodge of Freemasonry, the Premier Grand Lodge of England, was founded in London.1724 On the Feast of St. John the Baptist, Bach led the first performance of Christ unser Herr zum Jordan kam, BWV7, the third cantata of his chorale cantata cycle.1943 Amid racial tensions, U.S. Army military police shot and killed a black serviceman after a confrontation at a pub in Bamber Bridge, England.2010 Julia Gillard (pictured) was sworn in as the first female prime minister of Australia after incumbent Kevin Rudd declined to contest a leadership spill in the Labor Party.William Arnold (b.1587)John Lloyd Cruz (b.1983)Lisa (b.1987)Rodrigo (d.2000)More anniversaries: June 23June 24June 25ArchiveBy emailList of days of the yearAboutThe springbok (Antidorcas marsupialis) is a medium-

Lanka.1259: Treaty of Paris is signed between Louis IX and Henry IIIMain article: 1260s1260: Mongols first major war defeat in the Battle of Ain Jalut against the Egyptians.1260: Toluid Civil War begins between Kublai Khan and Ariq Bke for the title of Great Khan.1261: Byzantines under Michael VIII retake Constantinople from the Crusaders and Venice.1262: Iceland brought under Norwegian rule, with the Old Covenant.1265: Dominican theologian Thomas Aquinas begins to write his Summa Theologiae.1268: Fall of the Crusader State of Antioch to the Egyptians.Main article: 1270sThe opening page of one of Ibn al-Nafis' medical works. This is probably a copy made in India during the 17th or 18th century.1270: Goryeo dynasty swears allegiance to the Yuan dynasty.1270: The Zagwe dynasty is displaced by the Solomonic dynasty.1271: Edward I of England and Charles of Anjou arrive in Acre, starting the Ninth Crusade against Baibars.12721274: Second Council of Lyon attempts to unite the churches of the Eastern Roman Empire with the Church of Rome.1274: The Mongols launch their first invasion of Japan, but they are repelled by the Samurai and the Kamikaze winds.1274: The Tepanec give the Mexica permission to settle at the islet Cauhmixtitlan (Eagle's Place Between the Clouds)1275: Sant Dnyaneshwar who wrote Dnyaneshwari (a commentary on the Bhagavad Gita) and Amrutanubhav was born.1275: King Kertanegara of Singhasari launched Pamalayu expedition against Melayu Kingdom in Sumatra (ended in 1292).1277: Passage of the last and most important of the Paris Condemnations by Bishop Tempier, which banned a number of Aristotelian propositions1279: The Song dynasty ends after losing the Battle of Yamen to the Mongols.1279: The Chola Dynasty in Southern India officially comes to an end.Main article: 1280s1281: The Mongols launch their second invasion of Japan, but like their first invasion they are repelled by the Samurai and the Kamikaze winds.1282: Aragon acquires Sicily after the Sicilian Vespers.1284: Peterhouse, Cambridge founded by Hugo de Balsham, the Bishop of Ely.1284: King Kertanegara launches the Pabali expedition to Bali, integrating Bali into the Singhasari territory.1285: Second Mongol raid against Hungary, led by Nogai Khan.1289: The County of Tripoli falls to the Bahri Mamluks led by Qalawun.1289: Kertanegara insulted the envoy of Kublai Khan, who demanded that Java pay tribute to the Yuan Dynasty.[11][12]Main articles: 1290s and 1300sHommage of Edward I (kneeling), to the Philippe le Bel (seated). As duke of Aquitaine, Edward was a vassal to the French king.The Mamluk Dynasty comes to an end and is replaced by the Khalji dynasty.1290: By the Edict of Expulsion, King Edward I of England orders all Jews to leave the Kingdom of England.1291: The Swiss Confederation of Uri, Schwyz, and Unterwalden forms.1291: Mamluk Sultan of Egypt al-Ashraf Khalil captures Acre, thus ending the Crusader Kingdom of Jerusalem (the last Christian state remaining from the Crusades).1292: Jayakatwang, duke of Kediri, rebels and kills Kertanegara, ending the Singhasari kingdom.1292: Marco Polo, on his voyage from China to Persia, visits Sumatra and reports that, on the northern part of Sumatra, there were six trading ports, including Ferlec, Samudera and Lambri.[13]1292: King Mangrai founds the Lanna kingdom.1293: Mongol invasion of Java.[14] Kublai Khan of Yuan dynasty China, sends punitive attack against Kertanegara of Singhasari, who repels the Mongol forces.1293: On 10 November, the coronation of Nararya Sangramawijaya as monarch, marks the foundation of the Hindu Majapahit kingdom in eastern Java.1296: First War of Scottish Independence begins.1297: Membership in the Mazor Consegio or the Great Council of Venice of the Venetian Republic is sealed and limited in the future to only those families whose names have been inscribed therein.1299: Ottoman Empire is established under Osman I.1300: Islam is likely established in the Aceh region.1300: Aji Batara Agung Dewa Sakti founds the Kingdom of Kutai Kartanegara/Sultanate of Kutai in the Tepian Batu or Kutai Lama.1300: The Turku Cathedral was consecrated in Turku.[15]1300: Sri Rajahmura Lumaya, known in his shortened name Sri Lumay, a half-Tamil and half Malay minor prince of the Chola dynasty in Sumatra established the Indianized Rajahnate of Cebu in Cebu Island on the Philippine Archipelago.Alai Gate and Qutub Minar were built during the Mamluk and Khalji dynasties of the Delhi Sultanate.[16]Early 13th century Xia Gui paints Twelve Views from a Thatched Hut, during the Southern Song dynasty (now in Nelson-Atkins Museum of Art, Kansas City, Missouri).The motet form originates out of the Ars antiqua tradition of Western European music.Manuscript culture develops out of this time period in cities in Europe, which denotes a shift from monasteries to cities for books.Pecia system of copying books develops in Italian university-towns and was taken up by the University of Paris in the middle of the century.Wooden movable type printing invented by Chinese governmental minister Wang Zhen in 1298.The earliest known rockets, landmines, and handguns are made by the Chinese for use in warfare.The Chinese adopt the windmill from the Islamic world.Guan ware vase is made, Southern Song dynasty. It is now kept at Percival David Foundation of Chinese Art, London.1250 Cliff Palace, Mesa Verde, and other Ancestral Pueblo architectural complexes reach their apex[17]1280s Eyeglasses are invented in Venice, Italy.Late 13th century Night Attack on the Sanjo Palace is made during the Kamakura period. It is now kept at Museum of Fine Arts, Boston.Late 13th century Descent of the Amida Trinity, raigo triptych, is made, Kamakura period. It is now kept at the Art Institute of Chicago.The Neo-Aramaic languages begin to develop during the course of the century.Christianity in the 13th century^ "Samudra Pasai worthy to be world historical site". Republika Online. 2017-03-24. Retrieved 2020-01-24.^ Coeds, George (1968). Walter F. Vella (ed.). The Indianized States of Southeast Asia. trans.Susan Brown Cowing. University of Hawaii Press. ISBN978-0-8248-0368-1.^ "St. Thomas Aquinas". Catholic Encyclopedia. Retrieved 2023-12-09.^ Brooks, Christopher (2020). Western Civilization: A Concise History. NSCC Libraries Pressbooks.^ Lee, Kenneth B. (1997). Korea and East Asia: The Story of a Phoenix. Greenwood Publishing Group. ISBN9780275958237.^ "Greater London, Inner London Population & Density History". www.demographia.com. Retrieved 2023-02-10. Quoting from The London Encyclopedia, Ben Weinreb and Christopher Hibbert, ed., Macmillan, 2010, ISBN1405049251^ Van Cleve, T. C. (1972). The Emperor Frederick II of Hohenstaufen: Immuntator Mundi. Oxford. p.143. ISBN0-198-22513-X.^ Kantorowicz, Ernst (1937). Frederick the Second, 11941250. New York: Frederick Ungar. p.228.^ "Ken Angrok". Encyclopdia Britannica. Retrieved 25 July 2010.^ Weinstein, Richard A.; Dumas, Ashley A. (2008). "The spread of shell-tempered ceramics along the northern coast of the Gulf of Mexico" (PDF). Southeastern Archaeology. 27 (2). Archived from the original (PDF) on 2012-04-25.^ Grousset, Rene (1988), Empire of steppes, Wars in Japan, Indochina and Java, New Jersey: Rutgers University Press, p.288, ISBN0-8135-1304-9.^ Kahler, H. (December 31, 1981). Modern Times. Brill Archive. ISBN9004061967 via Google Books.^ "History of Aceh". Archived from the original on August 13, 2012.^ Weatherford, Jack (2004). Genghis khan and the making of the modern world. New York: Random House. p.239. ISBN0-609-80964-4.^ "Kenelle kellot soivat? Kiipe 360-videon avulla Turun tuomiokirkon torniin". Yle Uutiset (in Finnish). 2017-07-02. Retrieved 2023-02-10.^ "Qutb Minar and its Monuments, Delhi". UNESCO World Heritage Centre. Retrieved 2023-02-10.^ Berlo and Phillips, 275James J. Walsh (1907). "The Thirteenth: Greatest of Centuries". nd.edu. Archived from the original on 2017-03-01.Retrieved from " 4The following pages link to 13th century External tools(link counttransclusion countsorted list) See help page for transcluding these entriesShowing 50 items.View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500)Coin (links | edit)List of decades, centuries, and millennia (links | edit)Economy of Italy (links | edit)Imperialism (links | edit)Inca Empire (links | edit)Lavandula (links | edit)Levant (links | edit)Libro de los juegos (links | edit)History of Mali (links | edit)Romania (links | edit)Smelting (links | edit)20th century (links | edit)15th century (links | edit)16th century (links | edit)17th century (links | edit)18th century (links | edit)14th century (links | edit)1st century (links | edit)4th century (links | edit)12th century (links | edit)11th century (links | edit)1282 (links | edit)7th century (links | edit)10th century (links | edit)9th century (links | edit)8th century (links | edit)6th century (links | edit)5th century (links | edit)3rd century (links | edit)2nd century (links | edit)4th century BC (links | edit)1st century BC (links | edit)2nd century BC (links | edit)3rd century BC (links | edit)5th century BC (links | edit)6th century BC (links | edit)21st century BC (links | edit)11th century BC (links | edit)1299 (links | edit)1326 (links | edit)1359 (links | edit)1389 (links | edit)1154 (links | edit)1163 (links | edit)1160s (links | edit)1380 (links | edit)1141 (links | edit)1135 (links | edit)1204 (links | edit)7th century BC (links | edit)View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500)Retrieved from " WhatLinksHere/13th_century"Type of programmable logic deviceNot to be confused with Programmable Array Logic.PLA schematic exampleA programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented to produce an output. It has 2N AND gates for N input variables, and for M outputs from the PLA, there should be M OR gates, each with programmable inputs from all of the AND gates. This layout allows for many logic functions to be synthesized in the sum of products canonical forms.PLAs differ from programmable array logic devices (PALs and GALs) in that both the AND and OR gate planes are programmable. PAL has programmable AND gates but fixed OR gates [clarification needed]In 1970, Texas Instruments developed a mask-programmable IC based on the IBM read-only associative memory or ROAM. This device, the TMS2000, was programmed by altering the metal layer during the production of the IC. The TMS2000 had up to 17 inputs and 18 outputs with 8 JK flip-flops for memory. TI coined the term Programmable Logic Array for this device.[1]Preparation in SOP (sum of products) form.Obtain the minimum SOP form to reduce the number of product terms to a minimum.Decide the input connection of the AND matrix for generating the required product term.Then decide the input connections of the OR matrix to generate the sum terms.Decide the connections of the inversion matrix.Program the PLA.PLA block diagram:1st block2nd block3rd block4TH block5th blockInput bufferAND matrixOR matrixInvert/non-invert matrixFlip-flop output bufferThe desired outputs for each combination of inputs could be programmed into a read-only memory, with the inputs being driven by the address bus and the outputs being read out as data. However, that would require a separate memory location for every possible combination of inputs, including combinations that are never supposed to occur, and also duplicating data for "don't care" conditions (for example, logic like "if input A is 1, then, as far as output X is concerned, we don't care what input B is": in a ROM this would have to be written out twice, once for each possible value of B, and as more "don't care" inputs are added, the duplication grows exponentially); therefore, a programmable logic array can often implement a piece of logic using fewer transistors than the equivalent in read-only memory. This is particularly valuable when it is part of a processing chip where transistors are scarce (for example, the original 6502 chip contained a PLA to direct various operations of the processor[2]).One application of a PLA is to implement the control over a datapath. It defines various states in an instruction set, and produces the next state (by conditional branching). [e.g. if the machine is in state 2, and will go to state 4 if the instruction contains an immediate field; then the PLA should define the actions of the control in state 2, will set the next state to be 4 if the instruction contains an immediate field, and will define the actions of the control in state 4]. Programmable logic arrays should correspond to a state diagram for the system.The earliest Commodore 64 home computers released in 1982 (into early 1983) initially used a programmed Signetics 82S100 PLA, but as the demand increased, MOS Technology / Commodore Semiconductor Group began producing a mask-programmed PLA, which bore part number 906114-01.[3]Field-programmable gate arrayGate arrayProgrammable Array Logic^ Andres, Kent (October 1970). A Texas Instruments Application Report: MOS programmable logic arrays. Texas Instruments. Bulletin CA-158.^ How MOS 6502 Illegal Opcodes really work^ arcadecomponents.com - Commodore 906114-01 64 PLA IC"Programmable Logic Array (PLA)". cmsc311. University of Maryland. 2003. Archived from the original on 2017-12-14."PLA (programmable logic array)". Java Applet. University of Hamburg. Archived from the original on 2013-01-15. Retrieved 2010-04-07.Retrieved from " A Programmable Logic Array therefore, comprises of a PLA chip having a fixed wiring structure of AND gates followed by OR gates that can be programmed. PLA is a type of programmable logic device to construct a reconfigurable digital circuit on its architecture. It includes memory as well as logical operation which enable the user to instruct the device to perform certain operations of logic. As indicated by many authors, PLAs themselves are not configured with a specific function at the time of manufacturing and are configured before use.What is Programmable Logic Array?A Programmable Logic Array (PLA) is the implementation of the combinational logic circuits using a programmable type of a digital logic device. There is a programmable AND gate array with a programmable OR gate inputted thereafter, a feature that enables users to specify the required custom logic. PLAs tend to be more versatile due to their capability of being programmed to operate multiple logic functions and hence can be used in the designing of specific hardware solutions.Comparison with other Programmable Logic DevicesPLA has a programmable AND gate array and programmable OR gate array.PAL has a programmable AND gate array but a fixed OR gate array.ROM has a fixed AND gate array but programmable OR gate array.PLA is similar to a ROM in concept; however, it does not provide full decoding of variables and does not generate all minterms as in the ROM. Though its name consists of the word "programmable", it does not require any type of programming like in C and C++.Features of Programmable Logic ArrayProgrammable AND and OR Gates: PLA has two types of arrays, namely programmable AND gate array and programmable OR gate array so that the logic circuits can be designed in any way.Reconfigurability: As compared with other logic devices, the operation of PLAs is highly flexible and these devices may be easily programmed to perform any of the numerous logical functions.Partial Minterm Generation: It is also to be noted here that PLA does not provide the full decoding of variables like ROM but it functions only the necessary minterms.Combination of Memory and Logic: PLA has both the memory and the logic features hence making it suitable for various applications.Basic Block Diagram for PLAFollowing Truth table will be helpful in understanding function on no of inputs:ABCF1F2000000010001000011101000110111110001111F1 = AB'C' + ABC' + ABCon simplifying we get : F1 = AB + AC'F2 = A'BC + AB'C + ABCon simplifying we get: F2 = BC + ACFor the realization of the above function following circuit diagram will be used.PLA is used for the implementation of various combinational circuits using a buffer, AND gate, and OR gate. In PLA, all the minterms are not realized but only required minterms are implemented. As PLA has a programmable AND gate array and a programmable OR gate array, it provides more flexibility but the disadvantage is, it is not easy to use.The Operation of a PLA can be Summarized in Three Steps1. Programming: The user defines the logic function to be implemented by the PLA by programming the input and output configurations into the device.2. Product term generation: The inputs are applied to the AND gate array to produce a set of product terms.3. Sum term generation: The product terms are then applied to the OR gate array to generate the final output.PLAs are often used in digital systems as they are versatile and allow complex functions to be implemented easily. They are particularly useful for implementing Boolean expressions with many variables as the arrays of AND gates and OR gates can be configured to handle large numbers of inputs.Applications of Programmable Logic ArrayPLA is used to provide control over datapath.PLA is used as a counter.PLA is used as a decoder.PLA is used as a BUS interface in programmed I/O.Advantages of Programmable Logic ArrayFlexibility: Both the programmable AND gates and also the programmable OR gates offer the beneficial benefits of being used in a number of combinational circuits.Efficient Minterm Usage: It will only implement the necessary minterms thus making the design compact and more efficient.Reconfigurability: The PLAs can be reconfigured to perform different logic functions depending with the requirements of an application.Disadvantages of Programmable Logic ArrayComplexity: PLAs are slightly different from other programmable logic devices due to their high flexibility that makes the usage of PLAs a little complicated.Cost: It has higher cost as compared to the least complex logic devices such as PALs but it offers programming and flexible control.ConclusionProgrammable Logic Arrays (PLAs) are one of the typical categories of programmable devices, offering the possibility to construct variable digital systems. Being equipped with their programmable AND and OR gates, the functionality of PLAs is to implement several types of combinational logic functions are present. These are employed in many incidences like control over datapath, counters, decoder, and BUS interfaces. As it is evident, HDFSs have many advantages over other storage technologies; however, they are more complicated and costly, and are not as convenient as solutions with a relatively lower level of sophistication. Programmable Logic Arrays (PLAs) are an essential component in digital electronics, offering flexibility and efficiency in implementing combinational logic circuits. This article delves into the architecture, functionality, applications, advantages, and limitations of PLAs, providing a thorough understanding of their role in modern electronics. What is a Programmable Logic Array (PLA)?A PLA is a type of programmable logic device that consists of two levels of logic gates, an AND plane followed by an OR plane. Both levels are programmable, allowing for the implementation of complex combinational logic functions. PLAs are known for their ability to be customized for specific logic operations, making them highly versatile in various digital circuits. Architecture of a PLAThe architecture of a PLA can be broken down into the following components:Input Buffers: These are used to interface the PLA with external signals, ensuring proper voltage levels and signal integrity.AND Plane: This is the first level of logic gates in a PLA. It consists of a programmable array of AND gates that generate product terms based on the input variables.OR Plane: The second level of logic gates, consisting of a programmable array of OR gates. These gates sum the product terms generated by the AND plane to produce the desired output functions.Output Buffers: These interface the PLAs outputs with the external circuitry, ensuring the proper voltage levels and driving capabilities. How PLAs WorkThe functionality of a PLA can be understood through its two main operations:Programming the AND Plane: The inputs are fed into the AND plane, where each AND gate can be programmed to generate a specific product term (a combination of input variables). The programmability allows for creating any combination of the input variables.Programming the OR Plane: The product terms generated by the AND plane are fed into the OR plane. Each OR gate can be programmed to sum specific product terms, resulting in the desired output logic functions. Applications of PLAsPLAs are used in a variety of applications due to their flexibility and reconfigurability:Custom Logic Implementation: PLAs are ideal for implementing custom logic circuits where off-the-shelf components are unsuitable.State Machines: Used in designing finite state machines for control applications in digital systems.Address Decoding: Employed in memory address decoding in microprocessor systems.Signal Processing: Utilized in digital signal processing applications where specific logic functions need to be implemented. Advantages of PLAsFlexibility: PLAs can be reprogrammed to implement different logic functions, making them highly adaptable to changing requirements.Reduced Component Count: By integrating multiple logic functions into a single device, PLAs reduce the need for multiple discrete logic components, simplifying circuit design.Customizability: PLAs allow for custom logic designs tailored to specific applications, providing a high degree of design freedom. Limitations of PLAsComplexity: Programming PLAs can be complex and requires specialized tools and knowledge.Limited Speed: PLAs may not be as fast as other dedicated logic devices, such as FPGAs, for certain high-speed applications.Power Consumption: The programmability of PLAs can lead to higher power consumption compared to fixed-function logic devices. ConclusionProgrammable Logic Arrays (PLAs) play a crucial role in digital electronics, offering flexibility and efficiency in implementing custom logic functions. Their architecture, consisting of programmable AND and OR planes, allows for the creation of complex combinational logic circuits tailored to specific applications. While they have certain limitations, such as complexity and power consumption, their advantages make them invaluable in various digital design scenarios. Understanding PLAs and their applications is essential for anyone involved in the field of digital electronics and circuit design.

Explain programmable logic array. Programming logic array. What is the purpose of a programmable logic array pla). Define programmable logic array. What is programmable logic array. Programble logic array.